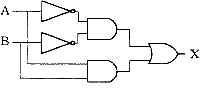
CME 2003 LOGIC DESIGN -

MDTERM EXAM

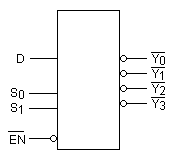
1. The BCD number for decimal 473 is
   1. 111011010
   2. 110001110011
   3. 010001110011
   4. 010011110011
2. A positive-going pulse is applied to an inverter. The time interval from the leading edge of the input to the leading edge of the output is 7 ns. This parameter is
   1. Speed-power product
   2. Propagation delay, tPHL
   3. Propagation delay, tPLH
   4. Pulse width
3. A single-precision floating-point binary number has a total of
   1. 8 bits
   2. 16 bits
   3. 24 bits
   4. 32 bits
4. Which one of the following is *not* a valid rule of Boolean algebra?
   1. 
   2. 
   3. 
   4. 
5. According to DeMorgan’s theorems, the following equality(s) are incorrect:
   1. 
   2. 
   3. 
   4. None of them
6. An example of a standard SOP expression is
   1. 
   2. 
   3. 
   4. All of them
7. The OR operation can be produced with
   1. Three NAND gates
   2. Two NAND gates
   3. One NOR gate
   4. Three NOR gates
8. All Boolean expressions cannot be implemented with
   1. NAND gates only
   2. NOR gates only
   3. Combinations of AND and OR gates
   4. Combinations of AND gates and inverters
9. The Gray code 10011011 is equal to the binary number
   1. 11010110
   2. 01100100
   3. 11101101
   4. 10011011
10. For the SOP expressionhttp://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq4_01800.gif , how many 0s are in the truth table's output column?
    1. 1
    2. 3
    3. 5
    4. 8
11. What is the difference between setup time and hold time?
    1. Setup time occurs after the active clock edge, hold time occurs before the active clock edge.
    2. Setup time occurs before the active clock edge, hold time occurs after the active clock edge.
    3. Setup time and hold time both occur at the active clock edge.
    4. None of them
12. How many 3-line-to-8-line decoders are required for decoding a 6-bit binary number?
    1. 4
    2. 5
    3. 6
    4. 8
13. Which statement below best describes a Karnaugh map?
    1. Karnaugh map can be used to replace Boolean rules.
14. The Karnaugh map eliminates the need for using NAND and NOR gates.
15. Variable complements can be eliminated by using Karnaugh maps.
16. Karnaugh maps provide a visual approach to simplifying Boolean expressions.

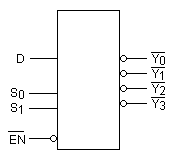
1. The implementation of simplified sum-of-products expressions may be easily implemented into actual logic circuits using all universal \_\_\_\_\_\_\_\_ gates with little or no increase in circuit complexity. (Select the response for the blank space that will BEST make the statement true.)
   1. AND
   2. NAND
   3. NOR
   4. OR
2. When adding an even parity bit to the code 110010, the result is \_\_\_\_\_\_\_\_.
   1. 1110010
   2. 1111001
   3. 110011
   4. 0110010
3. Which gate is best used as a basic comparator?
   1. A. NOR
   2. OR
   3. Exclusive-OR
   4. AND
4. What type of logic circuit is represented by the figure shown below?
   1. XOR
   2. XAND
   3. XNOR
   4. XNAND
5. How many (2 or 3 inputs ) gates would be required to implement the following Boolean expression before simplification? XY + X(X + Z) + Y(X + Z).
   1. 4
   2. 5
   3. 6
   4. 7
6. What is the primary motivation for using Boolean algebra to simplify logic expressions?
   1. It may make it easier to understand the overall function of the circuit.
   2. It may reduce the number of gates.
   3. It may reduce the number of inputs required.
   4. all of the above
7. Use Boolean algebra to find the most simplified SOP expression for F = ABD + CD + ACD + ABC + ABCD.
   1. F = ABD + ABC + CD
   2. F = CD + AD
   3. F = BC + AB
   4. F = AC + AD
8. Occasionally, a particular logic expression will be of no consequence in the operation of a circuit, such as a BCD-to-decimal converter. These result in \_\_\_\_\_\_\_\_terms in the K-map and can be treated as either \_\_\_\_\_\_\_\_ or \_\_\_\_\_\_\_\_, in order to \_\_\_\_\_\_\_\_ the resulting term.
   1. don't care, 1s, 0s, simplify
   2. spurious, ANDs, ORs, eliminate
   3. duplicate, 1s, 0s, verify
   4. spurious, 1s, 0s, simplify
9. Each "1" entry in a K-map square represents:
   1. a HIGH for each input truth table condition that produces a HIGH output.
   2. a HIGH output on the truth table for all LOW input combinations.
   3. a LOW output for all possible HIGH input conditions.
   4. a DON'T CARE condition for all possible input truth table combinations.
10. The carry propagation can be expressed as \_\_\_\_\_\_\_\_.
11. Cp = AB
12. Cp = A + B
13. Cp = A ⊕ B
14. Cp = (A ⊕ B)’
15. A decoder can be used as a demultiplexer by \_\_\_\_\_\_\_\_.
    1. tying all enable pins LOW
    2. tying all data-select lines LOW
    3. tying all data-select lines HIGH
    4. using the input lines for data selection and an enable line for data input
16. How many 4-bit parallel adders would be required to add two signed binary numbers each representing decimal numbers up through 12010?
    1. 2
    2. 3
    3. 4
    4. 5
17. Convert the following SOP expression to an equivalent POS expression.

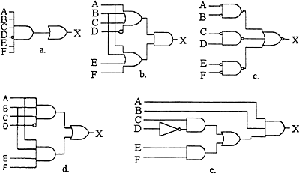
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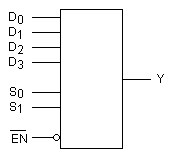
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| |  |  | | --- | --- | | [a)](javascript:%20void%200;) | http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mca4_0160a.gif | | [b)](javascript:%20void%200;) | http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mca4_0160b.gif | | [c)](javascript:%20void%200;) | http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mca4_0160c.gif | | [d)](javascript:%20void%200;) | http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mca4_0160d.gif | |

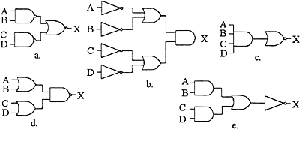
1. An AND gate with schematic "bubbles" on its inputs performs the same function as a(n)\_\_\_\_\_\_\_\_ gate.
   1. NOT
   2. OR
   3. NAND
   4. NOR



1. The device shown here is most likely a \_\_\_\_\_\_\_\_.
2. comparator
3. multiplexer
4. demultiplexer
5. parity generator
6. The NAND or NOR gates are referred to as "universal" gates because either:
   1. can be found in almost all digital circuits
   2. can be used to build all the other types of gates
   3. are used in all countries of the world
   4. were the first gates to be integrated
7. Which of the following statements accurately represents the two BEST methods of logic circuit simplification?
   1. Karnaugh mapping
   2. Waveform analysis
   3. Truth table
   4. Boolean algebra
8. Two 4-bit binary numbers (1011 and 1111) are applied to a 4-bit parallel adder. The carry input is 1. What are the values for the sum and carry output?
   1. Σ3Σ2Σ1Σ0=0111, Cout = 0
   2. Σ3Σ2Σ1Σ0=1111, Cout = 1
   3. Σ3Σ2Σ1Σ0=1011, Cout = 1
   4. Σ3Σ2Σ1Σ0=1100, Cout = 1
9. The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?
   1. A > B = 1, A < B = 0, A < B = 1
   2. A > B = 0, A < B = 1, A = B = 0
   3. A > B = 1, A < B = 0, A = B = 0
   4. A > B = 0, A < B = 1, A = B = 1
10. For the device shown here, assume the D input is LOW, both S inputs are HIGH, and the http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq6_01801.gifinput is HIGH. What is the status of the http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq6_02101.gifoutputs?
11. All are HIGH.
12. All are LOW.
13. All but http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mca6_0210c.gifare LOW.
14. All but http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mca6_0210c.gif are HIGH.
15. Which segments of a seven-segment display would be required to be active to display the decimal digit 2?
    1. a, b, d, e, and g
    2. a, b, c, d, and g
    3. a, c, d, f, and g
    4. a, b, c, d, e, and f
16. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(tot)) is \_\_\_\_\_\_\_\_.
    1. 12 ms
    2. 17 ns
    3. 48 ns
    4. 60 ns
17. How many data select lines are required for selecting eight inputs?
    1. 1
    2. 2
    3. 3
    4. 4
18. Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



1. For the device shown here, let all D inputs be LOW, both S inputs be HIGH, and the http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq6_01801.gif input be LOW. What is the status of the Y output?
   1. LOW
   2. B. HIGH
   3. C. Don't Care
   4. D. Cannot be determined
2. Convert BCD 0001 0010 0110 to binary.
   1. 1111110
   2. 1111101
   3. 1111000
   4. 1111111
3. The priority encoder has ten active-HIGH inputs and four active-HIGH outputs. What would be the state of the four outputs if inputs 4 and 5 are HIGH and all other inputs are LOW?
   1. A3=0, A2=1,A1=0,A0=1
   2. A3=1, A2=1,A1=0,A0=1
   3. A3=1, A2=0,A1=1,A0=0
   4. A3=0, A2=0,A1=1,A0=1
4. Which of the figures in figure (a to d) is equivalent to figure (e)?



1. Which of the following circuit parameters would be most likely to limit the maximum operating frequency of a flip-flop?
   1. setup and hold time
   2. clock pulse HIGH and LOW time
   3. propagation delay time
   4. clock transition time
2. The term *bit* means
   1. A small amount of data
   2. A 1 or a 0
   3. Binary digit
   4. Both answers (b) and (c)
3. Synchronous (parallel) counters eliminate the delay problems encountered with asynchronous (ripple) counters because the:
   1. input clock pulses are applied only to the first and last stages.
   2. input clock pulses are applied only to the last stage.
   3. input clock pulses are applied simultaneously to each stage.
   4. input clock pulses are not used to activate any of the counter stages.
4. The time interval on the leading edge of a pulse between 10% and 90% of amplitude is the
   1. Rise time
   2. Fall time
   3. Pulse width
   4. Period
5. The truth table for the SOP expression http://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq4_01900.gif has how many input combinations?
   1. 2
   2. 4
   3. 6
   4. 8
6. A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is \_\_\_\_\_\_\_\_.
   1. constantly LOW
   2. constantly HIGH
   3. a 20 kHz square wave
   4. a 10 kHz square wave
7. For the SOP expressionhttp://www.indiabix.com/_files/images/digital-electronics/digital-fundamentals/mcq4_01900.gif , how many 1s are in the truth table's output column?
   1. 1
   2. 2
   3. 3
   4. 4
8. Edge-triggered flip-flops must have:
   1. very fast response times.
   2. at least two inputs to handle rising and falling edges.
   3. a pulse transition detector.
   4. active-LOW inputs and complemented outputs
9. How many flip-flops are required to make a MOD-32 binary counter?
   1. 3
   2. 45
   3. 5
   4. 32
10. What is one disadvantage of an S-R flip-flop?
    1. It has no enable input.
    2. It has an invalid state.
    3. It has no clock input.
    4. It has only a single output
11. Which of the following is correct for a gated D flip-flop?
    1. The output toggles if one of the inputs is held HIGH.
    2. Only one of the inputs can be HIGH at a time.
    3. The output complement follows the input when enabled.
    4. Q output follows the input D when the enable is HIGH.
12. The Boolean expression is
    1. A sum term
    2. A literal term
    3. A product term
    4. Both answers (a) and (c)
13. The Boolean expression http://www.indiabix.com/_files/images/digital-electronics/basic-digital-electronics/mcq5_1031_1.gif is logically equivalent to what single gate?
    1. NAND
    2. NOR
    3. AND
    4. OR
14. In a certain digital waveform, the period is twice the pulse width. The duty cycle is
    1. 100%
    2. 200%
    3. 50%
    4. 150%
15. A ripple counter's speed is limited by the propagation delay of:
    1. each flip-flop
    2. all flip-flops and gates
    3. the flip-flops only with gates
    4. only circuit gates
16. The binary number 11011101 is equal to the decimal number
    1. 121
    2. 221
    3. 441
    4. 256
17. The decimal number -34 is expressed in the 2’s complement form as
    1. 01011110
    2. 10100010
    3. 11011110
    4. 01011101
18. A pulse in certain waveform occurs every 10ms. The frequency is
    1. 1 kHz
    2. 1 Hz
    3. 100 Hz
    4. 10 Hz
19. A pulse is applied to each input of an exclusive-OR gate. One pulse goes HIGH at t = 0 and goes back LOW at r = I ms. The other pulse goes HIGH at r = 0.8 ms and goes back LOW at t = 3 ms. The output pulse can be described as follows:
    1. It goes HIGH at t = 0 and back LOW at t = 3 ms.
    2. It goes HIGH at t = 0 and back LOW at r = 0.8 ms.
    3. It goes HIGH at t = I ms and back LOW at t = 3 ms.
    4. both answers (b) and (c)

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| ( 10 ) | **63** | Find single precision floating point number for the following **signed** hexadecimal value: **A980** |
| ( 20 ) | **64** | Design a combinational circuit which finds the remainder of division of BCD number by 3. The circuit has 4-bit input ( ABCD) and 2-bit output (XY).  number ***mod*** 3 = ? (the modulo operation)   1. Write the Boolean functions of the outputs X and Y 2. Draw the combinational circuit for the simplest form of the X function using only NAND gates. 3. The output function of X can be implemented by using 4-to-1 multiplexer? Show the circuit if it is possible. 4. Is it possible to implement the X output function if we have only 2 X 4 decoders and OR gates? |